



VGEN[®]

STIMULUS GENERATION LANGUAGE

WHAT IS VGEN?

VGEN is a stimulus generation language which reduces the time required to create, modify, document and maintain simulation stimulus files by up to **80%**! **VGEN** provides a powerful high-level language interface for the pattern generation task and runs on a variety of hardware platforms including SUN, HP-700, RS6000 and PC/AT.

With **VGEN**, a designer can define and document simulation stimulus patterns using powerful high-level language constructs which are tailored to the particular needs of simulators and testers. **VGEN** also allows substantial flexibility for modifying parameters that are important to simulators and testers. Principle features of **VGEN** include:

- Signal grouping (vectorizing)
- Subroutines with parameter passing
- Logical, arithmetic & shift operations for algorithmically generating patterns
- Pattern looping & conditional tests
- Reading data from external data files
- Data Tables
- Commenting for improved documentation & debugging
- Programmable Timing step, pin timing & time scaling
- Programmable Pin Types--NRZ, RZ, RO, RC, SBC, RX . . .
- Multiple time lines for parallel synchronous designs
- Method for defining expected results on output pins with link to **VCAP**
- Interfaces to over 30 popular simulators + user-definable output formats

Today's logic simulators offer substantial capability for doing comprehensive, accurate logic and timing simulation. **VGEN** is a tool which enables the designer to take full advantage of this capability. **VGEN** can also be used to specify expected state data for output pins which can then be used by **VCAP** to verify simulation results data.

WHY USE VGEN?

Design engineers today involved with ASIC or system-level design have become increasingly dependent upon CAE/CAD tools for the successful realization of their projects. Accuracy, completeness and timeliness are all important factors in achieving success. While many of the tools used today derive much of their effectiveness through the high-level of abstraction by which they allow the designer to work, the tools for stimulus generation remain primitive. The situation is analogous to requiring software developers to write code in machine language (1's & 0's) or at best in assembly language. **VGEN** is a high-level language stimulus *COMPILER* which elevates the designer's interface to the stimulus creation task and provides benefits for the designer similar to those that a high-level language gives a software developer.

ADVANTAGES:

- Provides program framework for hierarchical, modular development of test vectors.
- Provides facilities for algorithmic generation of test vectors.
- Provides very powerful facilities for defining and modifying pin timing.
- Provides facilities for dealing with asynchronous events and "parallel synchronous" circuits.
- Provides excellent documentation on vector set organization and flow.
- Interfaces to all popular simulators.

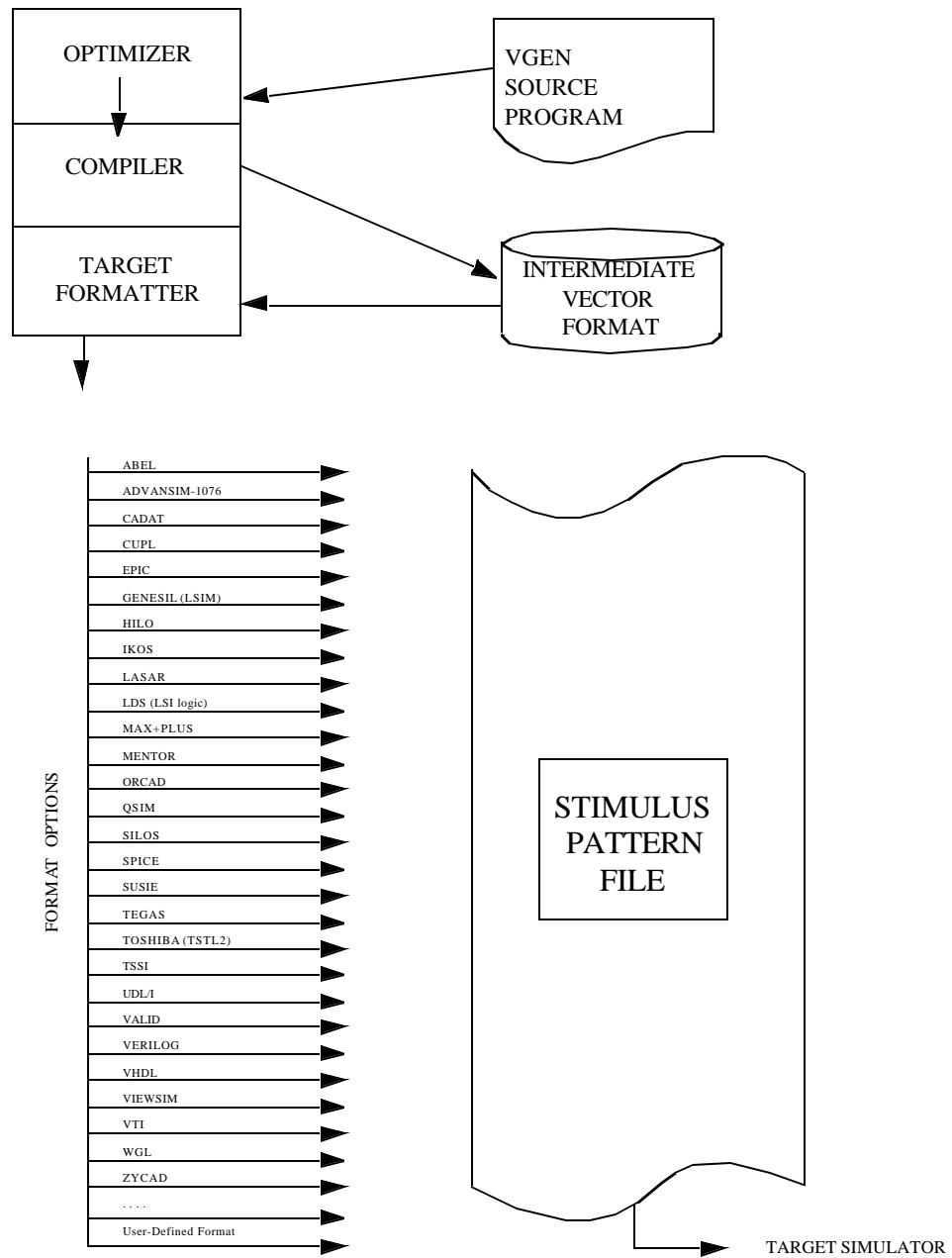
RESULTS:

- Substantially reduced development time for simulation stimulus vectors.
- Dramatically improved documentation of vectors which aids in modification, maintenance and translation to optimal test programs.
- Creation of vector sets which accurately emulate system timing resulting in more accurate and realistic simulation data.
- A single, powerful vector generation language can be learned and used to meet all of your stimulus vector creation needs--independent of logic simulator used.



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The VGEN compiler was developed with a primary goal of portability between platforms, operating systems and logic simulators. It is currently running on Sun SPARC, HP-700, IBM RS600 and PC/AT platforms under UNIX and MS-DOS operating systems. Building pattern files initially in an intermediate format results in the ability to cleanly interface to multiple simulators. Each of the more than 30 interfaces currently available is a separate, independent module, with new interfaces and interface options constantly being added.



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