



VCAP[®]

VECTOR COMPARISON AND ANALYSIS PROGRAM

VCAP is a comprehensive simulation data comparison and analysis program. When performing data comparisons, it provides powerful features for normalizing simulation data to adjust for differences in format, timing and print mode. Timing analysis on a simulation results file includes reporting output pin delays and transitions, input pin timing behavior, and a resource summary for checking tester compatibility.

APPLICATIONS

- **Verifying** simulation results data with **expected results** data. This expected results data may be from a VGEN source file or from virtually any other data source.
- **Comparing** simulation results data from **successive simulation runs**; for example, from a simulation run prior to physical layout with one after layout.
- **Comparing** simulation results data produced by **different logic simulators**. This need arises often when design methodologies utilize behavioral-level simulation and logic synthesis tools, when reference (or golden) simulators are required in the verification process.
- **Analyzing** simulation results data for pin behavior and timing. This is very useful for **checking tester compatibility** early in the design cycle.

VCAP is able to handle a wide range of input data formats using a collection of canned readers for popular formats or by letting the user define the format. This is done with single or multiple format descriptors which the user customizes to describe the input data format. Separate format descriptors can be used for results files from different simulators during data comparisons. Processing of the simulation results from different files can also be

used to normalize the data prior to comparison.

FEATURES

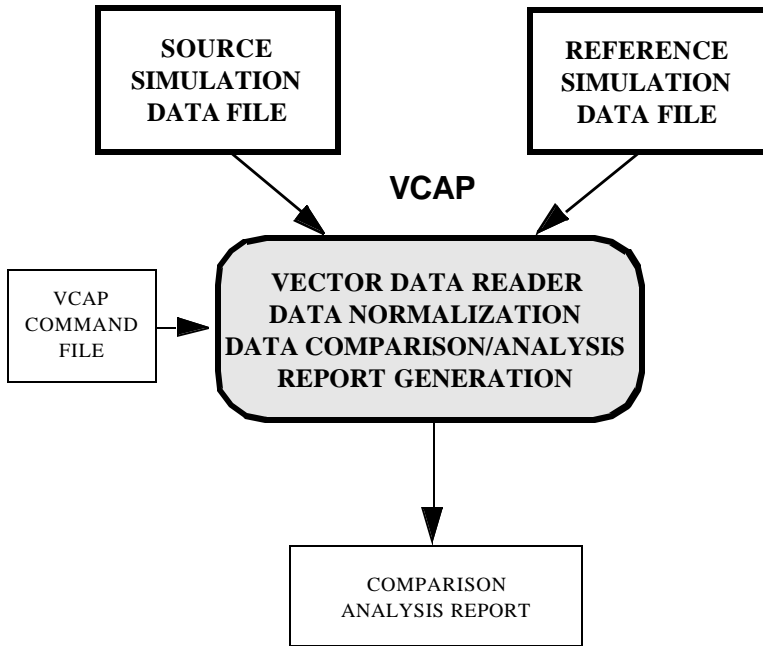
- **Canned readers** and a **User-Programmed reader** provide the capability of reading almost any simulation results data file.
- **Powerful data processing features** for normalizing simulation data from different simulators. These include state mapping, timing translation from print-on-change data to cycle data, and input/output data separation on bidirectional pins.
- Flexible, yet **powerful data comparison parameters** including: specifying which pins to compare, timing tolerances to be allowed during the comparisons, time zones during which to mask specified pins, and four different comparison algorithms from which to choose.
- **VCAP** can perform a **comprehensive pin behavior and timing analysis** on a simulation results file; generating a timing data sheet, transition statistics, illegal state and glitch checks, and the assignment of user-specified tester resources.

A by-product of the increasing complexities in today's typical ASIC or custom chip designs and the powerful CAE tools applied to these designs, is the generation of large quantities of simulation data. This data is intended to give designers an opportunity to validate their designs before committing to expensive fabrication cycles. These verification tasks may include checking output pin timing, checking output pin states against expected states (or against the results of a different simulation run) and making sure that the simulation data file can be easily mapped to the desired tester. **VCAP** is a flexible, powerful CAE tool which can be utilized in almost any CAE environment to specifically address these important tasks.



3941 Park Drive, Suite 20-342
El Dorado Hills, CA 95762
(916) 941-9403 (916) 941-9404 FAX
<http://www.sourceiii.com>

VCAP VECTOR COMPARISON AND ANALYSIS PROGRAM

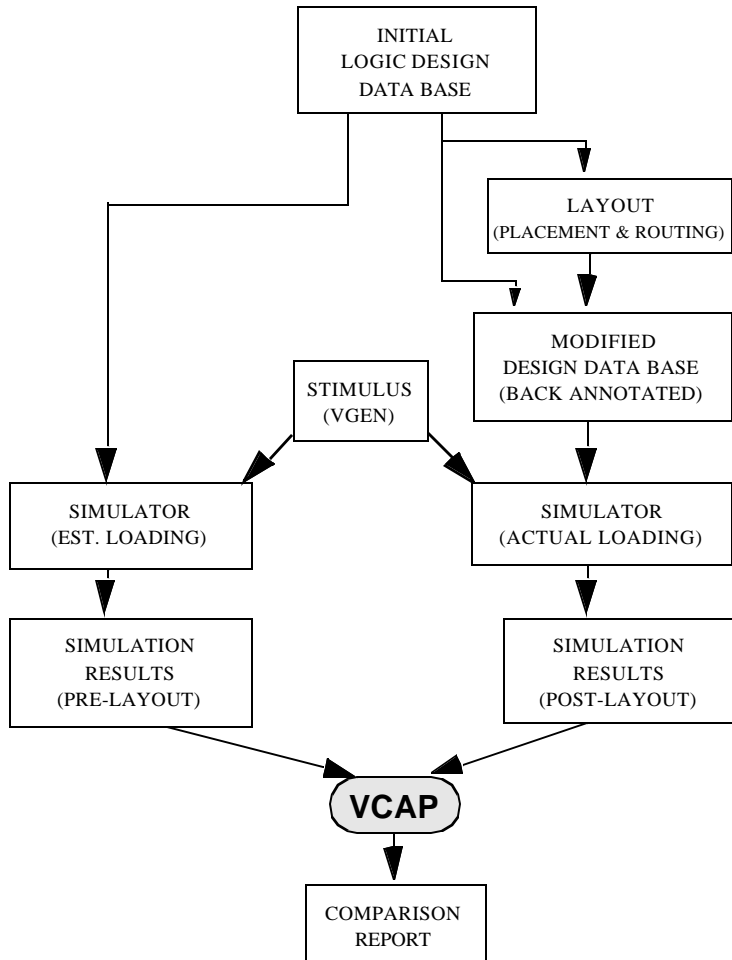


Upon invocation, **VCAP** reads the specified command file to determine the simulation data files it is to load and the tasks it is to perform. These tasks fall into two general categories; data file comparisons and data file analysis. In the command file, when doing data file comparisons, a reference and source file are identified, the data formats of the two files are separately defined, required normalization processing is described and the comparison parameters are defined. When doing analysis of a simulation results data file, the command file again identifies the source data file and the format of its data. In addition, the analysis parameters are defined. **VCAP** produces a report containing min/max delays for outputs, transition statistics and the identification of tester resources needed to accurately emulate the vector patterns and strobe the output states.

VCAP

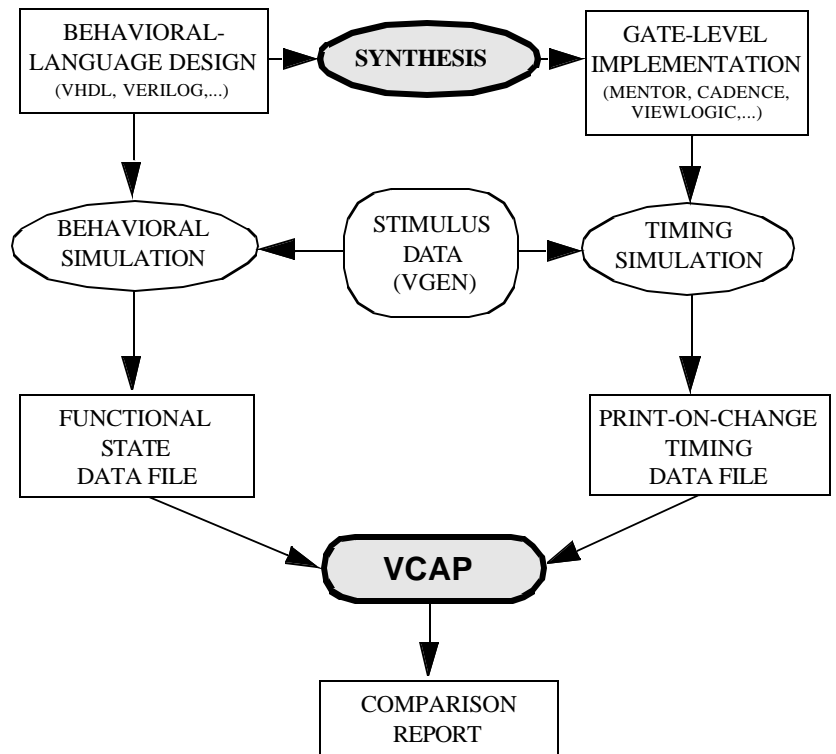
PRE & POST LAYOUT CHECK APPLICATION

In a typical ASIC or custom design flow, an important design verification point occurs when a final design data base is submitted to layout. Following layout, the actual loading on all signals is determined, this information is back-annotated to the design and a final post-layout simulation run is made. It is critical here that the newly generated (more accurate) simulation data set be verified to match (within appropriate timing tolerances) the original (pre-layout) simulation data. **VCAP** provides the timing tolerance and format flexibility to easily accomplish this verification.

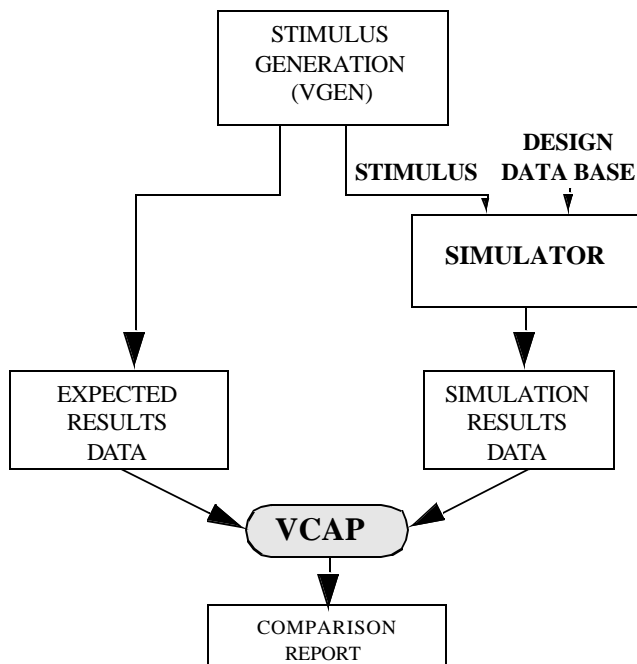


VCAP APPLICATION WITH SYNTHESIS TOOLS

Logic Synthesis tools currently available offer a high-level front-end to ASIC and custom design efforts. These tools allow designers to define their designs in an abstract behavioral language, without concern for implementation details, and then automatically produce a gate-level version for a specific foundry. In the design flow illustrated, two sets of simulation data are generated; one which is primarily state information from the behavioral simulation, and the other which contains detailed timing information from the gate-level simulation. **VCAP** can be very effectively utilized here to verify the synthesis process as well as checking spec. timing. **VCAP** reads the two data files of completely different formats, normalizing the data for timing and format differences, and then compares the results.



VCAP APPLICATION WITH VGEN® Verifying Simulation Results With Expected Results Data



VCAP can be used with **VGEN** to provide an automatic verification mechanism for checking simulation results against expected results. In this flow, the **VGEN** source file contains expected output state assignments, as well as input stimulus assignments. The expected output states can be defined as frequently, or as infrequently, as desired. The **VGEN** command **EXPECT_FILE** is used to cause all expected output data in the source file to be placed in a file separate from the input stimulus. Following Logic Simulation, **VCAP** is then directed to compare the Expected Results data with the output data from the Simulation results file. The timing for expected data can be set to the spec. limits in the **VGEN** source file so that the checking process will verify timing as well as state data. This verification methodology can be applied to virtually any CAE development environment.

TYPICAL VCAP COMPARISON REPORT

```
***** VCAP 2.0 COMPARE BLOCK REPORT *****

Date: Thu Feb  7 17:17:59 PST 2002
Source File: src
Reference File: ref

DON'T CARE STATES = `XT'
CYCLE = 100 NS
MAXIMUM NUMBER OF MISCOMPARES = 125
COMPARE TYPE = STATE, STATE

CHECK PIN NAME           SKEW TOLERANCE           MASK REGION
-----
cclk                     + 0.00 nS, - 0.00 nS
clk                      + 2.00 nS, - 2.00 nS
r/w                      + 2.00 nS, - 2.00 nS
ext                      + 0.00 nS, - 0.00 nS
db[7]                   + 0.00 nS, - 0.00 nS
db[6]                   + 0.00 nS, - 0.00 nS
db[5]                   + 0.00 nS, - 0.00 nS
db[4]                   + 0.00 nS, - 0.00 nS
rep*                    + 0.00 nS, - 0.00 nS

=====
VECTOR MISCOMPARE SUMMARY:

TIME          cc redddd r
              cl /xbbbb e
              lk wt[[[[ p
              k  7654 *
              ]]]]

53            REF: 00 11ZZZZ 1
              SRC: 00 01ZZZZ 1
              ^

220           REF: 10 00ZZZZ 0
              SRC: 11 00ZZZZ 0
              ^

Comparison Terminated Normally at : 18700
```

VCAP report files are created following the comparison or analysis of the specified vector files. The report file produced during comparison of two files includes all parameters relevant to the comparison process, as well as the mismatches found. When a file analysis is being performed, **VCAP** reports min/max rise and fall delays, transition statistics, and pin behavior.

SOURCE III provides a suite of CAE tools for dealing with the generation, translation and analysis of logic simulation data files. The software is available on most workstation platforms and interfaces to over 30 popular logic simulators.



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