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## CADENCE EXPANDS DESIGN CHAIN THROUGH ENCOUNTER TEST COLLABORATION WITH SOURCE III

Collaboration Enables Right-the-First-Time Test Conversion and Validation for Faster Time to Market and Improved Quality

SAN JOSE, Calif. , October 25, 2006

Cadence Design Systems, Inc. (NASDAQ: CDNS), the leader in global electronic-design innovation, and Source III, Inc., a leading developer of test conversion and verification programs, have announced a collaboration to enable improved test validation and faster test conversion for enhanced chip quality.

The joint effort expands the silicon design chain to include validation by Source III of test programs developed on the Cadence® Encounter® Test automated test program generation (ATPG) platform, as well as conversion of semiconductor test programs to targeted automatic-test-equipment (ATE) platforms.

Source III will validate test programs generated on the Encounter Test platform using Verilog model simulations as the golden standard. Additionally, Source III will convert and generate test programs from the Cadence standard test interface language STIL to a format readable by targeted ATE platforms.

"Our commitment at Source III is to reduce development cost, shorten time to market and deliver higher quality products," said John Cosley, president of Source III. "This collaboration with Cadence will provide design teams with new test methodologies to get to market faster and with improved quality."

"Cadence has enjoyed a long and mutually beneficial relationship with Source III," said Sanjiv Taneja, vice president of R&D for Encounter Test at Cadence. "As we expand the capabilities of Encounter Test to include features such as True-Time Test ATPG for small defect delay detection, team work such as this is critical to ensuring fast, high quality test results."

Cadence Encounter Test, a key component of the Cadence Encounter digital IC design platform, delivers the industry's most advanced test solution from RTL to silicon. Key technologies include Power-Aware ATPG methods to reduce power during test, test data compression to lower cost of test, True-Time delay test to detect small delay defects and enable highest-quality of shippable silicon and Encounter Diagnostics to accelerate yield ramp.

Encounter True-Time Test is available in L, XL and GXL configurations tailored to meet specific levels of testing complexity.

### About Cadence

Cadence enables global electronic-design innovation and plays an essential role in the creation of today's integrated circuits and electronics systems. Customers use Cadence software and hardware, methodologies, and services to design and verify advanced semiconductors, printed-circuit boards and systems used in consumer electronics, networking and telecommunications equipment, and computer systems. Cadence reported 2005 revenues of approximately \$1.3 billion, and has approximately 5,100 employees. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More information about the company, its products, and services is available at [www.cadence.com](http://www.cadence.com).

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